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EXAMINER	
NGUYEN, THANH T	
ART UNIT	**PAPER NUMBER**
2813	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/784,186	LIN ET AL.	
	Examiner	Art Unit	
	Thanh T. Nguyen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 20-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18, 20-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-18, 20-26 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 5-7 are stand rejected under 35 U.S.C. 102(b) as being anticipated by Wang et al. (U.S. Patent No. 5,679,606).

Referring to figures 2-6, Wang et al. teaches a method for gap filling between metal-metal lines, comprising:

providing a semiconductor structure, a surface of said semiconductor structure has a plurality of metal lines (14, see figure 2) thereon;

forming a first dielectric layer (22) on a surface and a side wall of said plurality of metal lines by a first high density plasma (ECR called high density plasma deposition, see figures 3, 6, col. 4, lines 62-67, col. 5, lines 1- col. 6, lines 1-20);

removing said first dielectric layer (22) until a portion of said side wall of said plurality of metal lines are exposed by a second high density plasma (ECR etching), wherein a portion of said first dielectric layer with a geometric shape is on some of said metal lines (14, see figures 3, 6, col. 6, lines 23-67)); and

forming a second dielectric layer (24/26) on said first dielectric layer by a third high density plasma (ECR)to fill gaps between the metal lines (14) and cover said plurality of metal lines and the portion of the first dielectric layer (22) with the geometric shape thereon to form an inter-metal dielectric layer (24/26, see figure 5, col. 7, lines 1-37) wherein all of the steps are performed in situ in a chamber (see col. 7, lines 32-36)..

Regarding to claims 5, 24, wherein the material of said plurality of metal lines is selected from the group consisting of AlCu alloy and Al alloy (see claim 4).

Regarding to claims 6, 25, wherein the material of said first dielectric layer is silicon dioxide (22, see col. 5, lines 7-8).

Regarding to claims 7, 26, wherein the material of said second dielectric layer is silicon dioxide (24/26, see claim 10, 11).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-4 are stand rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Patent No. 5,679,606) as applied to claim 1, 5-7 in view of Lee et al. (U.S. Patent No. 6,103,630), as previously applied.

Wang et al. teaches a method forming a gap filled metal lines. However, the reference does not teach forming an adhesive layer on the under side of the metal lines, forming an antireflection layer SiOxNy (ARC) on the metal line layer.

Lee et al. teaches a method forming an adhesive layer (32) on the under side of the metal lines (24), forming an antireflection layer SiOxNy (ARC, 26/28) on the metal line layer.

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would forming a metal lines with an adhesive layer on the under side of the metal and antireflection layer on top of the metal line layer in process of Wang et al. as taught by Lee et al. because antireflection layer would prevent the reflection of light and the adhesive layer would provide the adhesion between the metal line and the underlying layer.

Claims 8-18 are stand rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Patent No. 5,679,606) as applied to claim 1, 5-7 in view of Kim et al. (U.S. Patent Application Publication No. 2004/0119170).

Wang et al. teaches method for gap filling between metal-metal lines, comprising:

providing a first mixed gas in said chamber, wherein said first mixed gas comprises a first inert gas (argon), a first depositing gas (silane, SiH_4) and a first oxidative gas (oxygen, O_2, see col. 4, lines 62-67, col. 5, lines 1-67, col. 6, lines 1-21, meeting claims 9-10);

providing a second mixed gas in said chamber comprising argon (see col. 6, lines 23-67, meeting claim 14);

providing a third mixed gas in said chamber (ECR, see col. 7, lines 1-36), wherein said third mixed gas comprises a third inert gas (argon, see claim 9), a second depositing gas (silane) and a third oxidative gas (oxygen, see claim 9, meeting claims 16-18); and

However, the reference does not teach forming a semiconductor device by flowing first, second, and third mixed gas mixed gas in the chamber with both low frequency radio frequency power and high frequency radio power with a bias voltage on an electrostatic chuck, removing the first dielectric layer by argon and oxygen gas, the metal lines comprising an adhesive layer, and an antireflection layer of SiON.

Kim et al. teaches a method of forming a semiconductor device, forming a dielectric layer silicon oxide by using SiH_4 (depositing gas), O_2 (oxidative gas), and Ar (inert gas) in the chamber with both low frequency radio frequency power and high frequency radio power with a bias voltage on an electrostatic chuck, removing the first dielectric layer by using high density plasma (see paragraphs# 46-49), etching the first dielectric layer (SiO) by using argon (inert gas) and oxygen (oxidative gas, see paragraph# 41).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would flowing first, second, and third mixed gas mixed gas in the chamber with both low frequency radio frequency power and high frequency radio power with a bias voltage on an electrostatic chuck, removing the first dielectric layer by using high density plasma in process of Wang et al. as taught by Kim et al. because the process is known in the art to eliminate the formation of void on the surface of the dielectric layer, and etching the

first dielectric layer (SiO) by using inert gas and oxidative gas would provide desired etch selectivity.

Claims 20, 24-26 are stand rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Patent No. 5,679,606) in view of Hsu et al. (U.S. Patent Application Publication No. 2003/0211697).

Wang et al. teaches method for gap filling between metal-metal lines, comprising:

providing a semiconductor structure in a chamber (ECR chamber), wherein a surface of said semiconductor structure has a plurality of metal lines (14, see figure 2) thereon;

providing a first mixed gas in said chamber, wherein said first mixed gas comprises a first inert gas (argon), a first depositing gas (silane, SiH_4) and a first oxidative gas (oxygen, O_2, see col. 4, lines 62-67, col. 5, lines 1-67, col. 6, lines 1-21);

producing a first high density plasma from said first mixed gas to form a first dielectric layer (22) on a surface and a side wall of said plurality of metal lines (14, see figure 3, col. 4, lines 62-67, col. 5, lines 1-67, col. 6, lines 1-21););

providing a second mixed gas in said chamber (see col. 6, lines 23-67);

producing a second high density plasma from said second mixed gas to remove a portion of said first dielectric (22) later and a portion of said first dielectric layer with a geometric shape remains on some of said metal lines (14, see figure 3, 6, see col. 6, lines 23-67) ;

providing a third mixed gas in said chamber (ECR, see col. 7, lines 1-36), wherein said third mixed gas comprises a third inert gas (argon, see claim 9), a second depositing gas (silane) and a third oxidative gas (oxygen, see claim 9); and

producing a third high density plasma from said third mixed gas to form a second dielectric layer (24/26) on said first dielectric layer (22) to fill gaps between said metal lines (14) and cover said metal lines (14) and said portion of said first dielectric layer (22) with said geometric shape thereon to form an inter-metal dielectric layer wherein all of said steps are performed in situ in a chamber (see claim 9, col. 7, lines 1-36).

Regarding to claims 5, 24, wherein the material of said plurality of metal lines is selected from the group consisting of AlCu alloy and Al alloy (see claim 4).

Regarding to claims 6, 25, wherein the material of said first dielectric layer is silicon dioxide (22, see col. 5, lines 7-8).

Regarding to claims 7, 26, wherein the material of said second dielectric layer is silicon dioxide (24/26, see claim 10, 11).

However, the reference does not teach removing the first dielectric layer (SiO) by using inert gas and oxidative gas.

Kim et al. teaches a method of forming a semiconductor device, forming a dielectric layer silicon oxide by using SiH_4 (depositing gas), O_2 (oxidative gas), and Ar (inert gas) in the chamber with both low frequency radio frequency power and high frequency radio power with a bias voltage on an electrostatic chuck, removing the first dielectric layer by using high density plasma (see paragraphs# 46-49), etching the first dielectric layer (SiO) by using argon (inert gas) and oxygen (oxidative gas, see paragraph# 41).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would removing the first dielectric layer by using inert gas

and oxidative gas in high density plasma in process of Wang et al. as taught by Kim et al. because the process would provide desired etch selectivity.

Claims 20, 24-26 are stand rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Patent No. 5,679,606) in view of Hsu et al. (U.S. Patent Application Publication No. 2003/0211697).

Wang et al. teaches method for gap filling between metal-metal lines, comprising:

providing a semiconductor structure in a chamber (ECR chamber), wherein a surface of said semiconductor structure has a plurality of metal lines (14, see figure 2) thereon;

providing a first mixed gas in said chamber, wherein said first mixed gas comprises a first inert gas (argon), a first depositing gas (silane, SiH_4) and a first oxidative gas (oxygen, O_2, see col. 4, lines 62-67, col. 5, lines 1-67, col. 6, lines 1-21);

producing a first high density plasma from said first mixed gas to form a first dielectric layer (22) on a surface and a side wall of said plurality of metal lines (14, see figure 3, col. 4, lines 62-67, col. 5, lines 1-67, col. 6, lines 1-21););

providing a second mixed gas in said chamber (see col. 6, lines 23-67);

producing a second high density plasma from said second mixed gas to remove a portion of said first dielectric (22) later and a portion of said first dielectric layer with a geometric shape remains on some of said metal lines (14, see figure 3, 6, see col. 6, lines 23-67) ;

providing a third mixed gas in said chamber (ECR, see col. 7, lines 1-36), wherein said third mixed gas comprises a third inert gas (argon, see claim 9), a second depositing gas (silane) and a third oxidative gas (oxygen, see claim 9); and

producing a third high density plasma from said third mixed gas to form a second dielectric layer (24/26) on said first dielectric layer (22) to fill gaps between said metal lines (14) and cover said metal lines (14) and said portion of said first dielectric layer (22) with said geometric shape thereon to form an inter-metal dielectric layer wherein all of said steps are performed in situ in a chamber (see claim 9, col. 7, lines 1-36).

Regarding to claims 5, 24, wherein the material of said plurality of metal lines is selected from the group consisting of AlCu alloy and Al alloy (see claim 4).

Regarding to claims 6, 25, wherein the material of said first dielectric layer is silicon dioxide (22, see col. 5, lines 7-8).

Regarding to claims 7, 26, wherein the material of said second dielectric layer is silicon dioxide (24/26, see claim 10, 11).

However, the reference does not teach removing the first dielectric layer (SiO) by using inert gas and oxidative gas.

Hsu et al. teaches the first dielectric layer (SiO) by using argon (inert gas) and oxygen (oxidative gas, see paragraph# 46).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would etch the first dielectric layer (SiO) by using inert gas and oxidative gas in process of Wang because the process would provide desired etch selectivity.

Claims 21-23 are stand rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Patent No. 5,679,606) in view of Hsu et al. (U.S. Patent Application Publication No. 2003/0211697) as applied to claims 20, 24-26 and further in view of Lee et al. (U.S. Patent No. 6,103,630).

Wang et al. in view of Hsu et al. teaches a method forming a gap filled metal lines. However, the reference does not teach forming an adhesive layer on the under side of the metal lines, forming an antireflection layer SiOxNy (ARC) on the metal line layer.

Lee et al. teaches a method forming an adhesive layer (32) on the under side of the metal lines (24), forming an antireflection layer SiOxNy (ARC, 26/28) on the metal line layer.

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would forming a metal lines with an adhesive layer on the under side of the metal and antireflection layer on top of the metal line layer in process of Wang et al. as taught by Lee et al. because antireflection layer would prevent the reflection of light and the adhesive layer would provide the adhesion between the metal line and the underlying layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, can be reached on (571) 272-1702. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

Thanh Nguyen
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TTN